Archives of Current Research International
6(2): 1-11, 2016; Article no.ACRI.30062
ISSN: 2454-7077

SCIENCEDOMAIN *international*
www.sciencedomain.org

An Investigation on Characteristics of GaN Based MOSFETs and Their Driving Circuits

C. T. Ma[1*] and Z. H. Gu[1]

[1]Department of Electrical Engineering, Applied Power Electronics Systems Research Group, College of EECS, National United University, #2 Lien-Da, Miaoli City 36063, Taiwan, R.O.C.

Authors' contributions

This work was carried out in collaboration between both authors. Author CTM conducted the study, carried out the construction of hardware setup for the experimental tests and analysis. Author ZHG searched the cited papers, managed the device data sheets and parameters. Both authors read and approved the final manuscript.

Article Information

DOI: 10.9734/ACRI/2016/30062
Editor(s):
(1) Preecha Yupapin, Department of Physics, King Mongkut's Institute of Technology Ladkrabang, Thailand.
Reviewers:
(1) Igori Wallace, University of Nigeria, Nigeria.
(2) Zhan Wang, Power Electronics Circuit Group Transphorm Inc. Goleta, USA.
Complete Peer review History: http://www.sciencedomain.org/review-history/17106

Original Research Article

Received 14th October 2016
Accepted 29th November 2016
Published 2nd December 2016

ABSTRACT

Gallium nitride (GaN) based semiconductor devices are expected to play an important role in developing the next-generation power converters. With some intrinsic features, e.g., low switching power loss and high breakdown voltage, GaN MOSFETs can be used to realize high power density and better efficiency power converters with ultra-high switching frequencies. This paper firstly reviews characteristics of GaN based high electron-mobility transistors, some selected published papers and technical reports regarding applications of GaN MOSFETs in various power electronic systems and key issues regarding driving requirements of GaN MOSFETs followed by introducing a number of physical considerations in designing driving circuits and the related ICs. It follows that two practical driving circuits are designed on a given output voltage parameters in this paper. To verify the feasibility and effectiveness of the proposed driving schemes a 300 W synchronous buck converter with the proposed GaN gate drivers is constructed and tested. Some measured results are presented with brief discussions.

Keywords: Gallium nitride; power conversion; driving circuit; synchronous buck converter.

**Corresponding author: Email: ctma@nuu.edu.tw;*

1. INTRODUCTION

In recent years, development of renewable energy based power generation and advanced power converting technologies have been regarded as important and urgent tasks in power engineering related fields. In the aspect of designing advanced power converters, feasible means to achieve higher efficiency and power density are the most concerned issues. In practice, if further increasing power converting efficiency is desired, using better semiconductor devices is a quick and valid approach. In most of the known converter circuitries, power semiconductor devices are mainly used as switches, which are usually Si based devices in the past few decades. In order to further decrease power loss both in switching and conduction periods, GaN based high electron-mobility transistor (HEMT) provides promising solutions. Although silicon carbide (SiC) may have a number of merits over GaN [1] in some specific applications, GaN is overall a better choice in designing various high-frequency power converters. The applications of GaN HEMTs started in about 2004 with depletion-mode RF transistors by Eudyna Corporation in Japan. Using GaN on silicon carbide (SiC) substrates, Eudyna successfully brought transistors into its products designed for targeting the RF market [2]. Based on the reports from the semiconductor manufacturing company, GaN HEMTs have been offered commercially since 2006, and have found a lot of immediate uses in various wireless infrastructure applications mainly due to their high efficiency and high voltage capabilities [3].

Basically, GaN based devices have several advantages over Si-based devices, including faster switching, lower conducting and switching loss, higher working temperature, higher voltage withstand capability [4]. It has been believed that these features can further increase the efficiency of the system and enlarge their application domain in high-power converter systems. However, because of the very fast switching speed, some parasitic inductances and capacitances could make the driving of GaN HEMT become a difficult task. In practice, the PCB layout and driving circuit design should be very careful to keep the parasitic parameters as small as possible [5]. In the open literature, many applications using GaN based device can be found. For example, various GaN based high-performance power converters are reported in [5-15], mixed signal and RF systems are demonstrated in [16], motor drive systems in [17] and [18], also the converters for hybrid electric vehicles is discussed in [19]. Following the introduction section, the basics of the GaN HEMT is introduced In Section 2. In Section 3, some commercially available GaN HEMT devices are reviewed. The unique driving requirement are addressed in section 4 followed by a detailed description of a proposed driving circuits given in section 5, in which some typical measured results are presented to demonstrate the effectiveness of the proposed driving schemes.

2. GAN HEMT BASICS

As addressed in the introduction section, GaN material offers relatively high band-gap energy, critical electric field for breakdown in the crystals, saturated drift velocity and electron mobility, typical parameters for GaN, SiC and Silicon are given in Table 1 [2].

Theoretically, GaN HEMTs can be fabricated in various processes. The schematic structure of AlGaN/GaN HEMT is shown in Fig. 1. Due to the two-dimensional electron gas (2DEG) feature in the conduction channel between AlGaN and GaN, the carrier mobility can be enhanced remarkably [16]. In the past, GaN devices are reliable only under low frequencies but they have become more reliable in higher frequencies these years, making them become very useful devices in high-power converter systems. To have clear picture of the GaN HEMTs fabrication methods, depletion-mode (D-mode), enhancement-mode (E-mode) and cascode structure are briefly reviewed in the rest of this section. For further details one can refer to [20].

Table 1. Material properties of GaN, SiC, and Silicon at 300 K

Properties*	GaN	Si	SiC
E_G(eV)	3.4	1.12	3.2
E_{BR}(MV/cm)	3.3	0.3	3.5
V_S(x 10^7 cm/s)	2.5	1.0	2.0
M(cm^2/Vs)	990-2000	1500	650

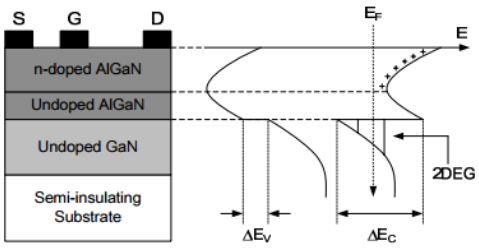

Fig. 1. Schematic structure of an AlGaN/GaN HEMT and the corresponding energy-band profile [16]

2.1 Depletion-mode GaN HEMT

A depletion-mode (D-mode) GaN HEMT is a normally-on device, because of its 2DEG, allowing current to flow through it without any gate voltage, which can become a problem if it is to be used as a switch. As a result, for applications in power conversion systems, D-mode GaN HEMTs are not popular. A schematic structure of a depletion-mode GaN HEMT is shown in Fig. 2 [20].

2.2 Enhancement-mode GaN HEMT

An enhancement-mode (E-mode) GaN HEMT is a normally-off device, because of a P-doped layer between gate and AlGaN layer, which can be either GaN or AlGaN, as shown in Fig. 3 [20]. E-mode GaN HEMTs are more commonly used as switches in designing power converting systems than Si MOSFETs for they provide zero Q_{rr}, smaller and more linear Q_{OSS} and lower gate charge Q_g.

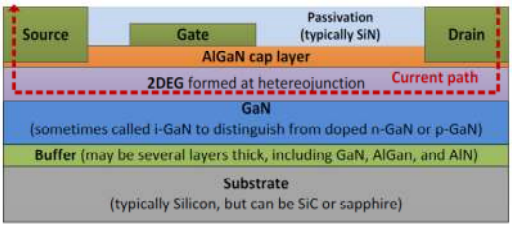

Fig. 2. Schematic structure of a D-mode GaN HEMT [20]

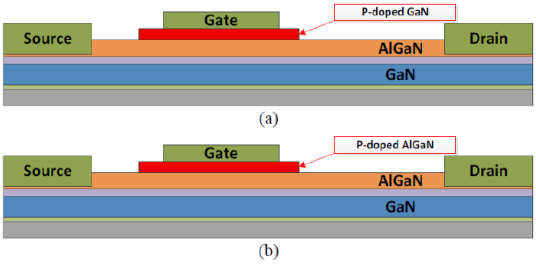

Fig. 3. Schematic structure of E-mode GaN HEMT [20]

In an E-mode GaN HEMT, when there's no voltage applied to gate (V_g=0), p-gate potential depletes the channel under the gate, resulting in no drain current; after $V_{GS(TH)}$ is applied, holes are injected and electrons generate accordingly, resulting in large drain current. The process is shown in Fig. 4.

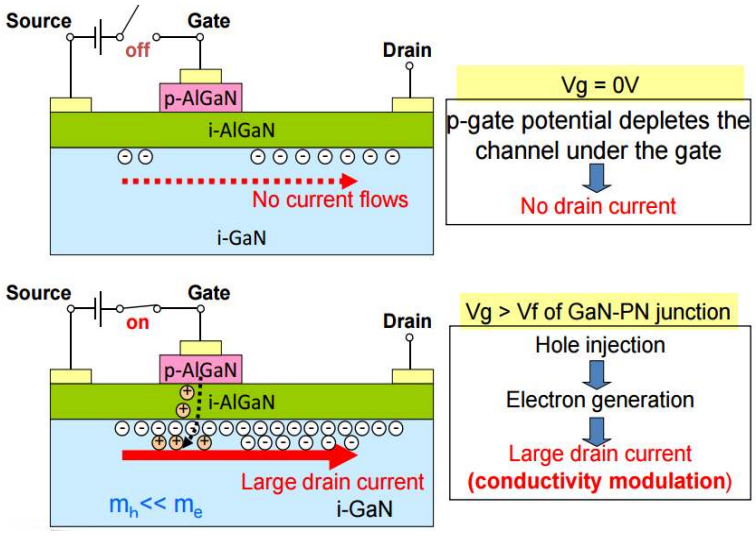

Fig. 4. Conduction of E-mode HEMT [20]

2.3 Cascode GaN HEMT

A cascode GaN FET is a native d-mode GaN HEMT and a low voltage Si FET in cascode structure, as shown in Fig. 6. Cascode GaN FET is easy to drive with off-the-shelf drivers. The driving task can be easily done by driving the LV Si FET with a normal gate driver, since the d-mode GaN HEMT has a normally-on status. Cascode GaN FETs have several advantages over E-mode GaN HEMT, in terms of easy gate drive, excellent body diode and almost zero Miller Effect. The conduction of a cascode GaN FET can be described as follows: when there's no voltage applied to gate (V_g=0), the low voltage Si MOSFET is off, and the D-mode GaN HEMT is on, resulting in the conduction of the body diode in the LV Si MOSFET and an overall reverse current if there's any; after $V_{GS(TH)}$ is applied, the LV Si MOSFET is on, which means the switch is on, resulting in large drain current. These processes are shown in Fig. 5.

3. GAN HEMT PRODUCTS

A list of commercially available high V_{GS} GaN HEMT products is shown in Table 2, which includes only the HEMT device with the highest V_{GS} and I_D ratings. Only GaN HEMTs that are enhancement-mode or in cascode structure are included in this list.

As mentioned above, GaN based power devices are much better than traditional Si based power devices. However, they are currently a relatively new technology, which means less availability in application experiences and higher price. Therefore, it is very important to carefully evaluate which devices to choose and also the way to drive these devices safely according to their specs given in datasheets. Some considerations for driving GaN HEMTs are discussed in the following section.

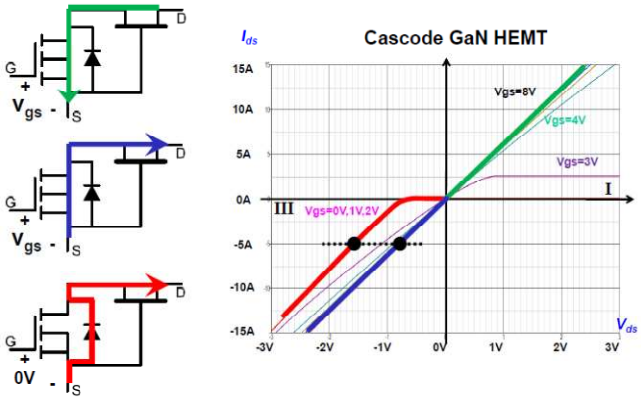

Fig. 5. Conduction of cascode GaN FET [20]

Table 2. Commercial high voltage GaN HEMTs products

Device number	Type	V_{rated} (V)	I_D (A)	$R_{DS(on)}$ (mΩ)	$V_{GS(th)}$ (V)	Q_g (nC)
1	E	300	6.3	90(typical) 120 (maximum)	-4~+6	1.8(typical) 2.3 (maximum)
2	E	600	15	71(25℃) 150(150℃)	-10~+4.5	--
3	E	650	7.5	200(typical) 260 (maximum)	-10~+7	1.5
4	Cascode	600	17(25℃) 12(100℃)	150(25℃) 340(150℃)	-18~+18	6.2(typical) 9.3 (maximum)
5	Cascode	650	50(25℃) 31.5(100℃)	35(25℃) 72(150℃)	-18~+18	28(typical) 42 (maximum)

4. GAN DRIVING CIRCUITS

A driving circuit makes a switching device turn on and off according to control signals, which is absolutely not a simple task when it comes to GaN based power devices because of the following reasons: high di/vt and dv/dt with the parasitic inductances and capacitances especially in leaded packages, which is currently the dominating package type used in the industry because of its convenience in PCB layout and heat sink arrangement. Theoretically, some GaN FETs are easy to use because its characteristics are similar to power MOSFETs, but their dissimilarities in high frequency applications can result in serious problems [20]. In practice, gate drive circuits can be made differently depending on the designer's consideration. However, some common factors in designing the driving circuits for the E-mode GaN HEMT and cascode GaN FET are briefly discussed in this section.

4.1 Driving Considerations for Enhancement-mode GaN HEMT

Enhancement-mode GaN HEMTs are normally-off, which means a driving signal is needed in order to turn it on. Most driving problems in an E-mode GaN HEMT are brought up by its ability to switch really fast, making a huge voltage transient with even a very small parasitic inductance. To drive an E-mode GaN HEMT safely, the following items must be carefully considered.

4.1.1 Optimizing gate resistors

E-mode GaN HEMT switching speed can be controlled by gate resistors, which is critical for optimum switching performance and gate drive stability. It is even better to separate R_G for turn-on and turn-off. $R_{G(on)}$ should be big enough to suppress gate ringing, lowering switching loss, and to avoid Miller turn-on and gate oscillation; $R_{G(off)}$ should be small enough to provide strong full-down for robust gate drive, as shown in Figs. 6 and 7 [21].

4.1.2 Preventing Miller turn-on

Designing a low pull-down impedance for the gate is a valid way to prevent Miller turn-on. It can be done by selecting a driver with low source R_{OL} or optimizing $R_{G(on)}$. Using a small $R_{G(off)}$ for turn-off or reducing the gate loop inductance L_G has a good result. Another way to do this is adding an external C_{GS}, providing additional Miller current shunt path, while this approach can slow down switching, increasing gate drive loss, and can be combined with parasitic inductance, yielding larger C_G. Another approach is adding negative gate voltage, typically -2V to -3V, is recommended. This method also reduces turn-off loss, while yielding higher reverse conduction loss. There are a few high side gate drive recommendations announced in the open literature, e.g., a full-isolated gate drive, which has the best performance with isolated power supply and minimizing inter-winding capacitance and bootstrap capability, which makes the overall cost lower, while post-regulation or voltage clamping is required.

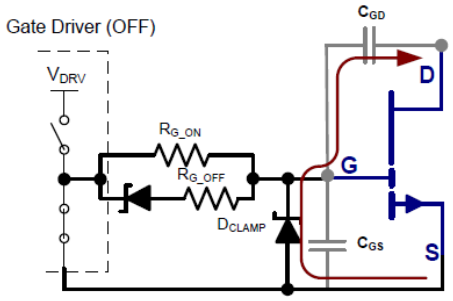

Fig. 6. Separate $R_{G(on)}$ and $R_{G(off)}$ with a clamping diode for a driver with single output [21]

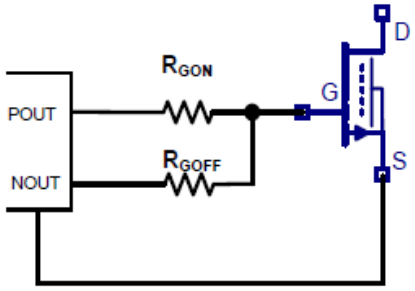

Fig. 7. Separate $R_{G(on)}$ and $R_{G(off)}$ for a driver with separate pull-up/down output [21]

4.1.3 Oscillation prevention

Oscillations could appear because of common source inductance L_{CS} feedback path from power loop to gate loop (di/dt) and the capacitive coupling via Miller capacitor C_{GD} (dv/dt). Therefore, L_{CS} and power loop inductance should be minimized. To prevent oscillations, one can reduce L_{CS}, L_G and minimize external C_{GD}; slow down turn-on to reduce dv/dt and gate ringing, reduce additional C_{GS}, which is a high frequency path for gate current ringing. Adding a small

ferrite bead in series with R_G is also a good suggestion.

4.2 Driving Considerations in Cascode GaN HEMT

Cascode GaN FETs are normally-off as E-mode GaN HEMTs, but there are several differences between these two types. The cascode GaN FET is compatible with standard FET gate driver and it has lower Q_G for a given current-handling capability. In addition, it is easier to achieve zero voltage switching (ZVS). However, there are a few disadvantages that requires special attention, e.g., $V_{GS(th)}$ of a cascode GaN FET is relatively low, which may easily result in fault turn-on. The common source inductance is a concern and the dv/dt could induce gate currents. To drive a high side cascode GaN FET, the following items must be considered [22].

4.2.1 Reference differences

The top switch has different reference with bottom switch. It is referenced to a floating ground, which swings from input voltage to ground at switching frequency, as shown in Fig. 8 blue line. The high dv/dt can appear in switching the GaN device at the V_{gST} turn-off moment, while V_{gSB} is referenced to power ground.

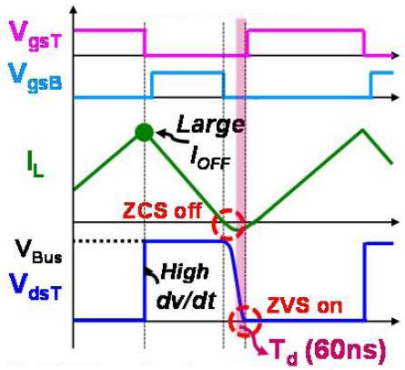

Fig. 8. Efficiency comparison between CRM ZVS and CCM hard switching [22]

4.2.2 High dv/dt

The dv/dt is normally very high at turn-off transition, which is usually over a few times higher than the state-of-the-art Si super junction MOSFET. This high dv/dt common-mode noise should be immune from the gate drive signal input side by a level-shifting circuit or isolation. Otherwise, the primary signal ground will be damaged by the high dv/dt noise through the input-output parasitic capacitance, C_{IO}. C_{IO} is the sum of capacitance coupled between the floating ground and the primary GND, which could include the capacitance of the isolation barrier, i.e., driver's transformer or the C_{IO} of the high-side isolated power supply.

4.2.3 High di/dt

Solving the high di/dt problem is also a challenge in driving circuit design. The result of a double pulse test shows that the di/dt in GaN device is around 8 times higher than Si SJ-MOSFET. Even a small common source inductance can introduce high voltage ringing in on and off transitions. Digital Isolator provides very small C_{IO} and high dv/dt immunity that can sustain over 100V/ns with careful design. The gate drive architecture with digital isolator for GaN is shown in Fig. 9. The softs witching fails with 200V/13.5A and dv/dt of 42V/ns, which is smaller than the typical value provided in the datasheet, 50V/ns, as shown in Fig. 10. This is possibly because C_{IO} is still too large for the test [22]. It is also found that the additional C_{IO} is because of a large switch and primary ground overlapping area within the two middle layers.

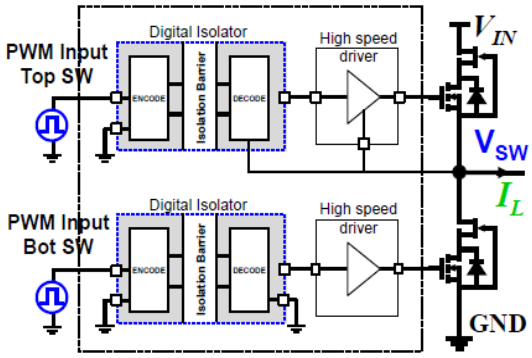

Fig. 9. Gate driver architecture with digital isolator for GaN [22]

5. THE IC PRODUCTS AND PROPOSED GAN HEMT DRIVERS

5.1 Driving IC Products

In this subsection, two effective driving circuits are proposed for GaN MOSTFETs. For reader's convenience, a list of commercially available drivers for GaN HEMT is shown in Table 3, which includes only the propagation time of the IC

family per manufacturer. This table also includes drivers that were originally designed for other types of transistors and were later found suitable for driving GaN HEMT.

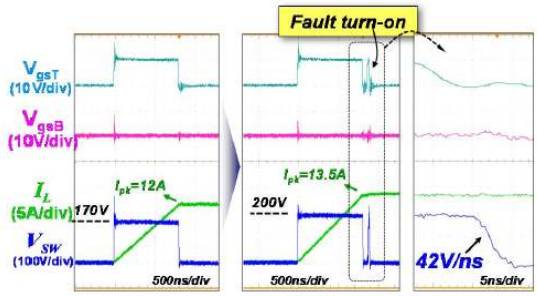

Fig. 10. The first single pulse test with digital isolator [22]

From the engineering point of view, the easiest and safest way to drive a specific GaN HEMT is to use a suggested deriving IC manufactured by its own company. Most GaN HEMT manufacturers suggest some suitable driving ICs to use with their own GaN HEMT devices. Since GaN related technologies are relatively new and it is believed that better and cheaper driver ICs will soon be available in the near future.

5.2 The Proposed GaN Driving Circuits

In this subsection, two driving circuits are addressed. The first circuit employs Si8230 as its main driving IC. Si8230 is normally used as an isolated precision half-bridge driver for IGBT and MOSFETs. This driver has the ability to drive up to two switches at the same time and provide the required signal isolation. This driver needs three floating DC voltage modules when driving two switches and two for driving one. The signal inputs can be either two complementary signals or one signal and its ground. When this driver serves as a gate driver for GaN It comes with signal isolation capability. Between the input VDD and GND, two bypass capacitors of 1uF are needed to provide a good high frequency bypassing path; between each output VDD and GND, two capacitors of 1uF and 10uF are also needed to provide large transient currents in switching transients. Ferrite beads might also be needed. Propagation delay of this circuit is estimated to be 60ns. The total price of ICs used in this circuit is around 1018 TWD (509 TWD per driver). The overall system block diagram is shown in Fig. 11.

The proposed second driving circuit employs ACPL-H343 as its main driving IC. This driver uses a different strategy to drive a GaN switch. The driving voltages, V_{GS} are set to be -3.3V to +14.7V or -5V to +13V. With a 15V non-floating DC source for both UC3845, a high performance current mode controller and DRV8800, a DMOS full-bridge motor driver, the two ICs combined yields a high frequency AC voltage, which is then transformed and rectified into a DC floating voltage of 18V. A zener diode keeps the capacitor voltage latched at 18V, which is for the V_{CC} of ACPL-H343. The other zener diode latches gating voltage of the GaN FET at +3.3V. The control PWM signals are sent to H343, whose output voltage changes from V_{CC} to V_{EE} with the frequency of the PWM signal. This proposed driving scheme allows the FET to be driven by a voltage that varies from negative voltage to positive voltage ranging from -3.3V to +14.7V. Propagation delay of this circuit is estimated at 350ns. The total price of ICs used in this circuit is around 314 TWD. It drives only one switch at a time. With four ICs used in this circuit, the overall system block diagram is shown in Fig. 12.

Table 3. Commercial GaN HEMT driver IC products

IC no.	Transistor type	Driving channels	Propagation delay (ns)
1	Power/SiC MOSFET	single	55
2	E-mode GaN FET	double	8.4
3	GaN FET	single	50
4	MOSFET	single	60
	IGBT		
	SiC FET		
	GaN FET		
5	E-mode GaN FET	double	28

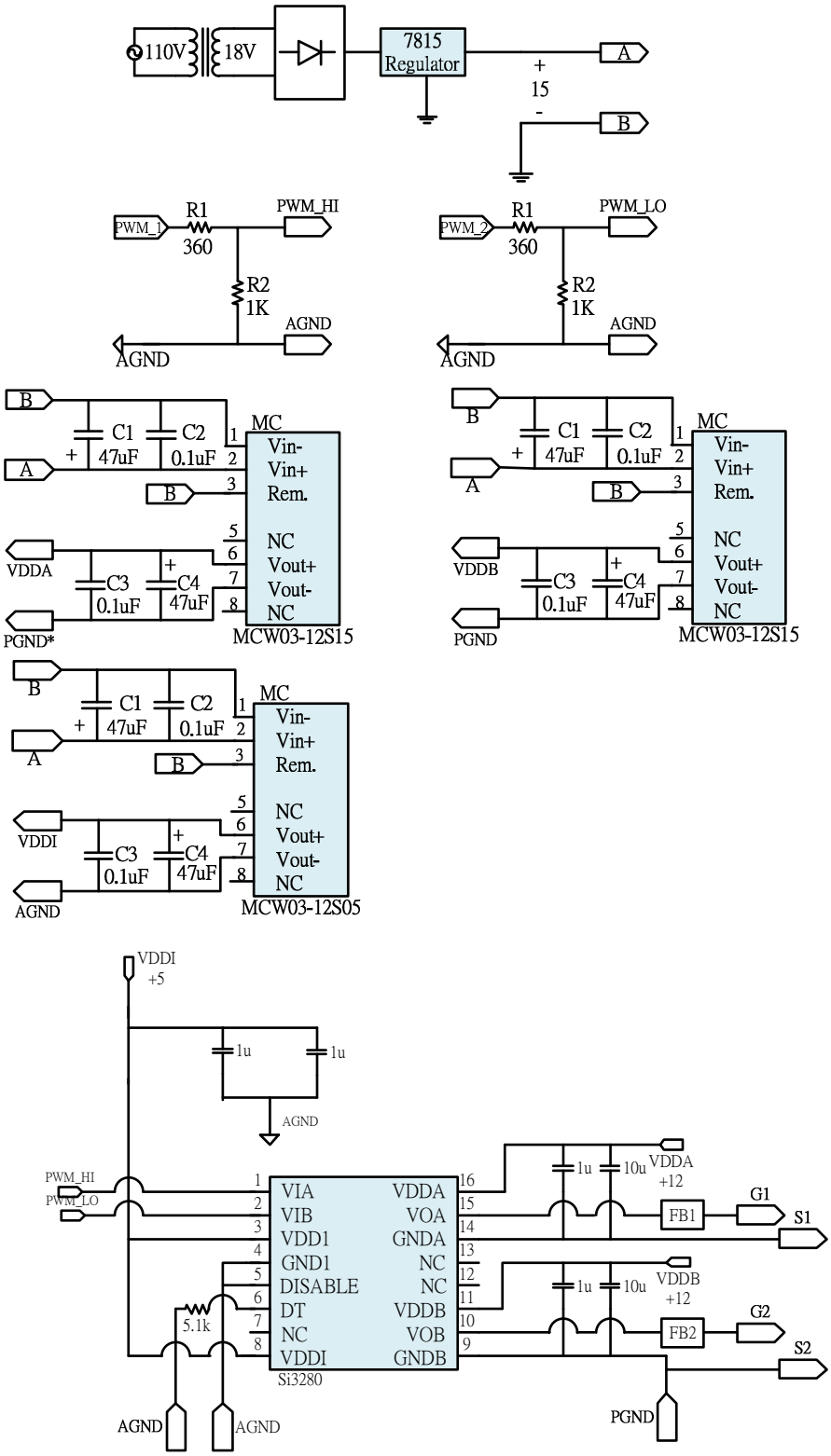

Fig. 11. The proposed first driving circuit

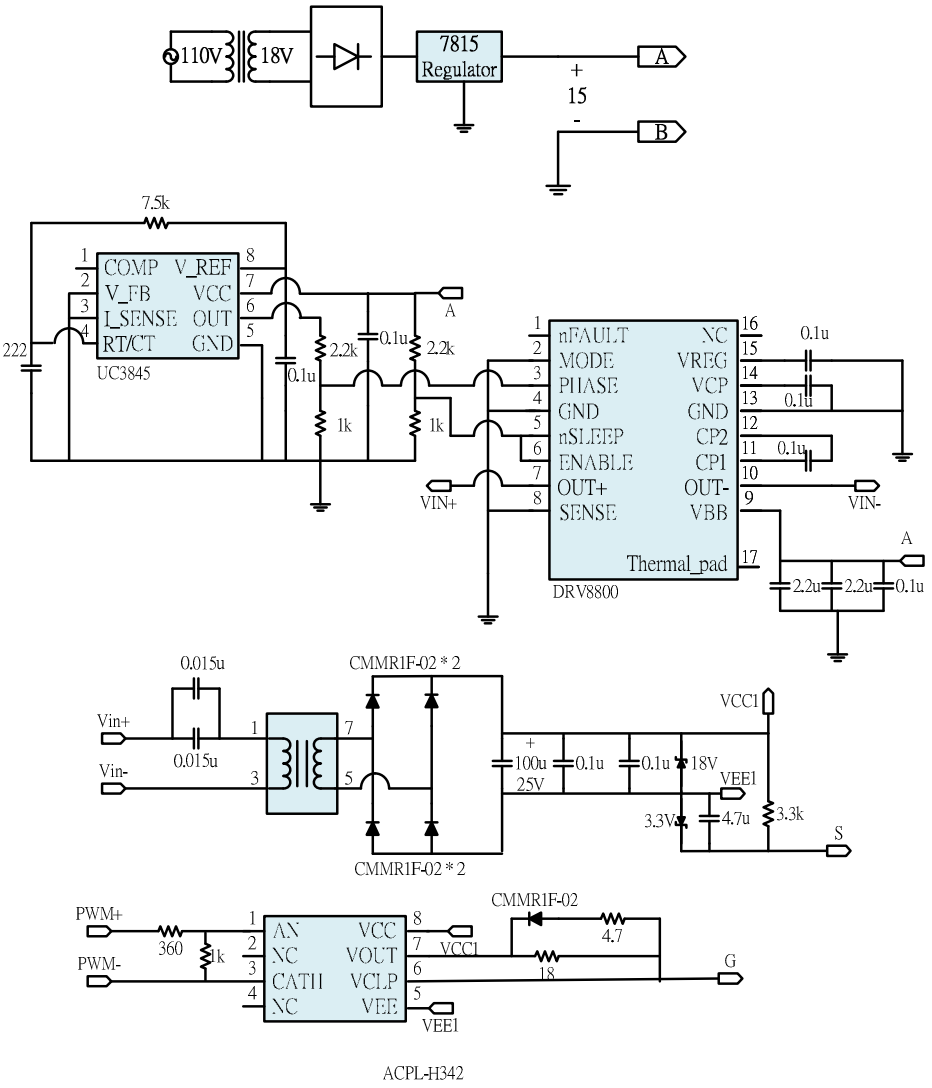

Fig. 12. The proposed second driving circuit

5.3 The Experimental Setup and Measured Results

For testing the proposed driving circuits, a 300 W synchronous buck converter using theTPH 3205WS as the power switches is constructed as shown in Fig. 13. The input voltage of the converter is set to be 20V to 36V and the output voltage is set to 12V for driving a 300W resistive load. A TI DSP 28335 is used as the main controller to perform a dual closed-loop voltage regulation. Since the main concern of this paper is focused on the performance of the proposed two GaN driving circuits the design details regarding the digital controllers are neglected for simplicity. In Fig. 14, the open-loop driving voltage waveform, Vgs (-5V to 13V) with a switching frequency of 100 kHz is shown. The Figs. 15 and 16 respectively show a set of measured waveforms of the two power switches working in the synchronous buck converter with the proposed two driving schemes mentioned in the previous subsection. Figs. 17 and 18 respectively show a set of he measured room-in switching waveforms of the power switch in the converter (turn on and turn off). As can be seen in the Figs. 15 and 16, both the proposed drivers are able to perform their driving tasks with satisfactory results; however, the proposed second driving circuit provides relatively better driving characteristics, in terms of driving speed and noise immunization.

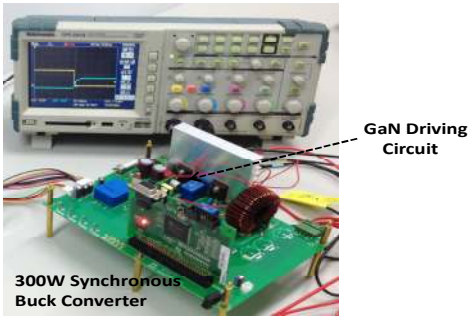

Fig. 13. A 300 W synchronous buck converter

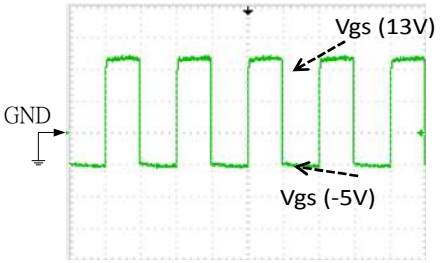

Fig. 14. The driving voltage waveform (Vgs, -5V to 13V, 100 kHz)

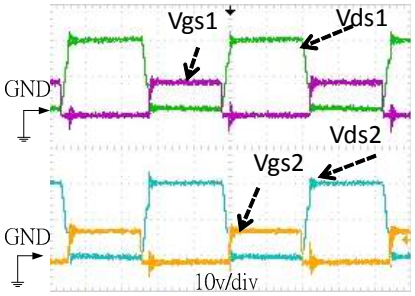

Fig. 15. The measured waveforms of the two power switches in the converter (the first driving circuit)

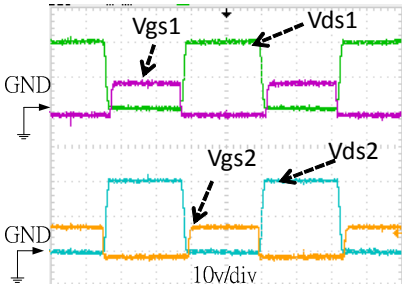

Fig. 16. The measured switching waveforms of the two power switches in the converter (the second driving circuit)

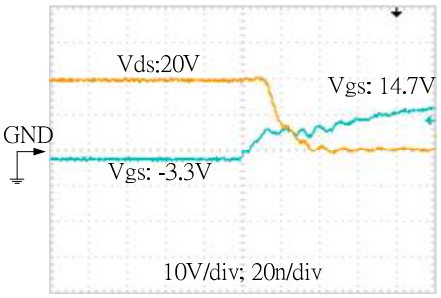

Fig. 17. The measured room-in switching waveforms of the power switch in the converter (turn-on)

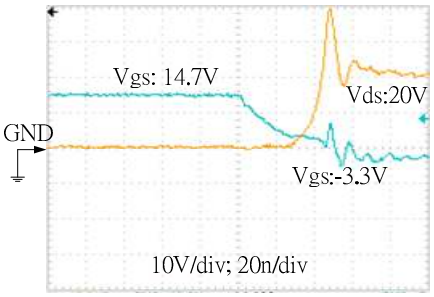

Fig. 18. The measured room-in switching waveforms of the power switch in the converter (turn-off)

6. CONCLUSION

GaN based power switches and their driving control schemes have become promising technologies in developing advanced power electronic systems for various industrial applications. It has been found that the main advantages GaN HEMT devices are high switching frequency, high breakdown voltage and very small reverse recovery charge. This paper has briefly reviewed on important issues regarding driving methods, possible application limits and conducting modes in GaN HEMTs including both normally on and normally off devices. A number of commercially available GaN devices along with their driving ICs are briefly discussed. The excellent features in GaN devices provide the possibility to design advanced power converter systems with higher efficiency and power density. In addition, to drive GaN HEMTs devices safely, the most concern issue is basically the treatment of their parasitic parameters. It should be noted that when the switching frequency is increased up to a certain level a false turn-on may occur even with very small parasitic inductance. In this paper, two driving schemes have been proposed and tested in a synchronous buck converter. Typical gating

and switching waveforms are measured and presented to verify the feasibility and effectiveness of the design drivers.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Mishra U. Compound semiconductor; GaN and SiC, separating fact from fiction in both research and business [C]. APEC Transphorm; 2013.
2. Lidow A, Strydom J, Rooij MD, et al. Gallium Nitride (GaN) technology overview [C].EDN network; 2012.
3. GaN applications. Available:https://en.wikipedia.org/wiki/Gallium_nitride#cite_note-22 (Access date: Sep. 2016)
4. McDonald T. GaN based power conversion moving on! [C]. IOR International Rectifier; 2013.
5. Wang Z, Wu YF, Honea J, et al. Paralleling GaN HEMTs for diode-free bridge power converters [C]. IEEE. 2015;1-7.
6. Wu YF. Paralleling high-speed GaN power HEMTs for quadrupled power output. [C]. IEEE. 2013;1-4.
7. Jenkins LL, Wilson CG, Moses JD, et al. The impact of parallel GaN HEMTs on efficienty of a 12-to-1 V buck converter. [C]. IEEE. 2013;1-4.
8. Xu Z, Zhang W, Xu F, et al. Investigation of 600 V GaN HEMTs for high efficiency and high temperature applications [C]. IEEE. 2014;1-6.
9. Saito W, Kuraguchi M, Takada Y, et al. High breakdown voltage undoped AlGaN–GaN power HEMT on sapphire substrate and its demonstration for DC–DC converter application [J]. IEEE Transactions on Electron Devices. 2004;51(11):1913-1917.
10. Hughes B, Yoon YY, Zehnder DM, et al. A 95% efficient normally-off GaN-on-Si HEMT hybrid-IC boost -converter with 425-W output power at 1 MHz [C]. IEEE. 2011;1-3.
11. Hayashi Y. Power density design of SiC and GaN DC–DC converters for 380 V DC distribution system based on series-parallel circuit topology [C]. IEEE. 2013;1-6.
12. Shenai K. High-frequency switching limitations in Gallium Nitride (GaN) and Silicon Carbide (SiC) power devices for boost converter applications [C]. IEEE. 2013;1-4.
13. Mitova R, Ghosh R, Mhaskar U, et al. Investigations of 600-V GaN HEMT and GaN diode for power converter applications [J]. IEEE Transactions on Power Electronics. 2014;29(5):2441-2452.
14. Maksimovi´c D, Zhang Y, Rodr´ıguez M. Monolithic very high frequency GaN switched-mode power converters [C]. IEEE. 2015;1-4.
15. Zhang Y. Very high frequency PWM buck converters using monolithic GaN half-bridge power stages with integrated gate drivers [J]. IEEE Transactions on Power Electronics. 2016;31(11):7926-7942.
16. WANG R. Enhancement /depletion-mode HEMT technology for III-Nitride mixed-signal and RF applications [C]. 2008;1-24.
17. Persson E, Raffo D. Appliance motor drive performance improvements using 600V GaN Cascode FETs [J]. PCIM Europe. 2014;330-337.
18. Wu YF, Kebort D, Guerrero J. High-frequency, GaN diode-free motor drive inverter with pure sine wave output [J]. Power Transmission Engineering. 2012; 40-43.
19. Ishiko M. Recent R & D activities of power device for hybrid eletric vehicles [J]. R&D Review of Toyota CRDL. 2004;39(4):1-6.
20. Persson E. Practical application of 600 V GaN HEMTs in power electronics [C]. IOR Infineon; 2015.
21. How to drive GaN enhancement mode HEMT. GaN Systems Inc., 26, April; 2016.
22. Zhang W, Huang X, Lee FC, et al. Gate drive design considerations for high voltage Cascode GaN HEMT [C]. IEEE; 2014.

Peer-review history:
The peer review history for this paper can be accessed here:
http://sciencedomain.org/review-history/17106